NARAYANA ENGINEERING COLLEGE::NELLORE

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

A REPORT ON **"Opportunities in VLSI Design"**

1	Name of the Activity/Event	Virtual Seminar on "Opportunities in VLSI Design"		
2	Date of Activity/Event	20/11/2021		
3	Organized by/Name of the committee	Dept. of Electronics & Communication Engineering		
4	Place of Activity/event	Narayana Engineering College, Nellore		
5	Resource person/guest/organization	Ms. Girija M.P Physical Design Engineer, SiValley Tech. Pvt. Ltd., Bangalore.		
6	Type of activity/Event	Virtual Seminar(IIIC)		
7	Activity/Event Objectives	1. To provide awareness about opportunities in VLSI Domain jobs. 2. Outline the various VLSI / Semiconductor companies. 3. To provide various job roles in semiconductor jobs.		
8	Participation	Students	Faculty	Total
		111	-	111
9	General remarks	The sessions are helpful to the students about various job roles in semiconductor jobs.		
10	Suggested Improvements	It would be useful if there is face to face interaction.		
11	Enclosures	1. Request letter 2. Circulars 3. Report 4. Attendance		
12	Signature of In charge/convener			

A BRIEF DESCRIPTION OF THE EVENT:

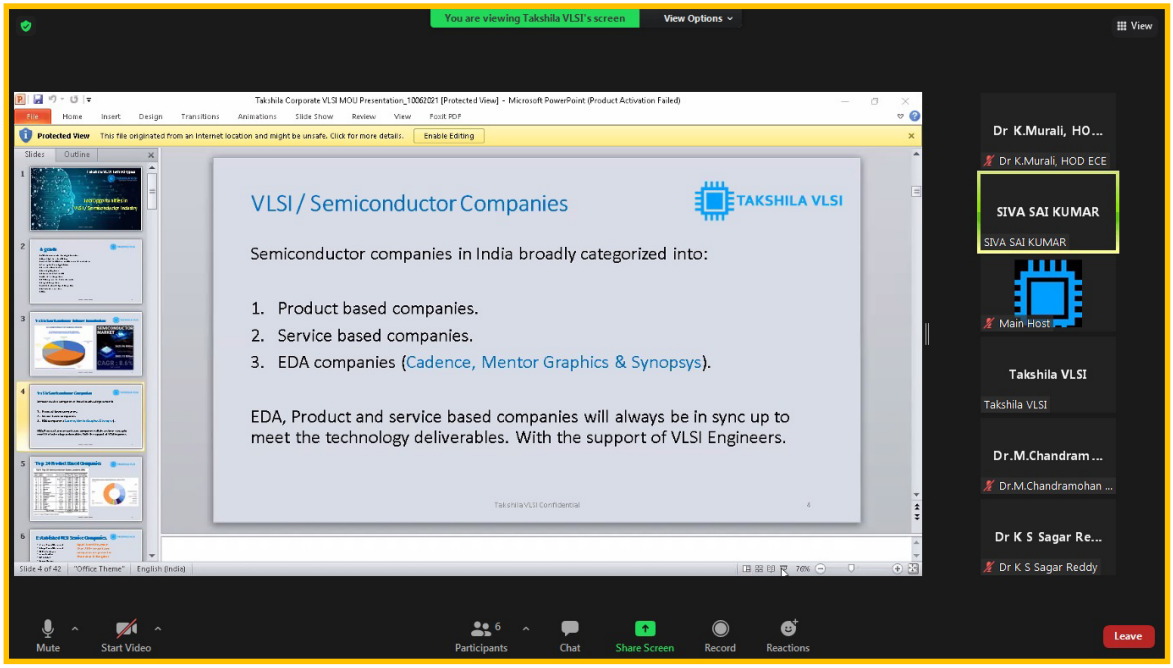
Department of Electronics and Communication engineering has conducted a virtual seminar on "Opportunities in VLSI Design" under IIIC for III B-Tech ECE students on 20-11-2021. The Resource Person for the event is Ms. Girija M.P, Physical Design Engineer, SiValley Tech. Pvt. Ltd., Bangalore.

The Head of the Department Dr. K. Murali inaugurated the session around 03:00 P. M. Dr. K. Murali Head of the ECE department initiated the session with motivating words and encouraged the students to be interactive during the session. The resource person given a brief introduction on VLSI / Semiconductor industry, eligibility criteria and various core job opportunities.

Figure: Introducing the resource person

The resource person started her lecture by explaining about the various categories in semiconductor companies. The various categories are as follows

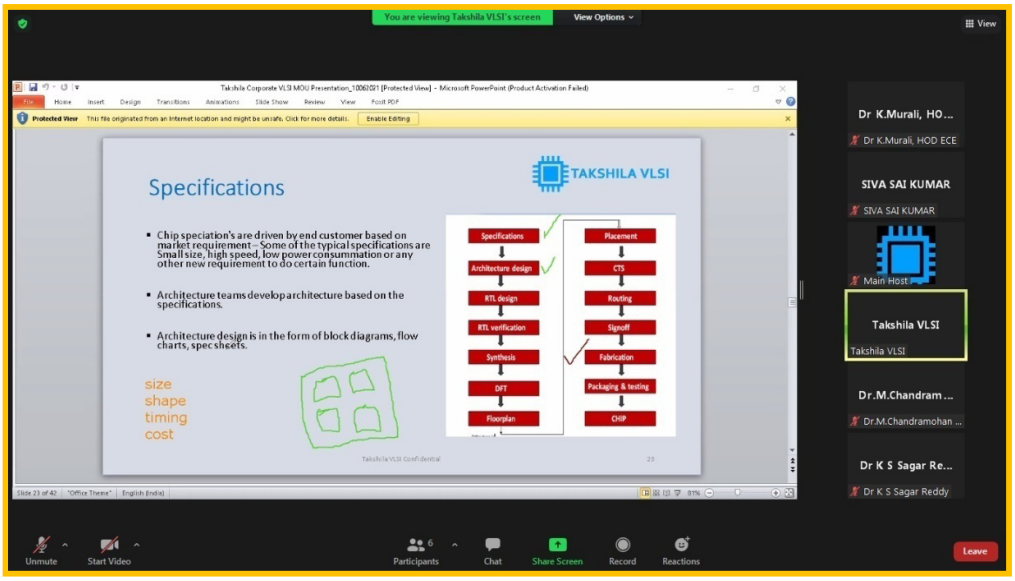
- Product based companies.
- Service based companies.
- EDA companies (Cadence, Mentor Graphics & Synopsys).



Explaining about categories in semiconductor companies.

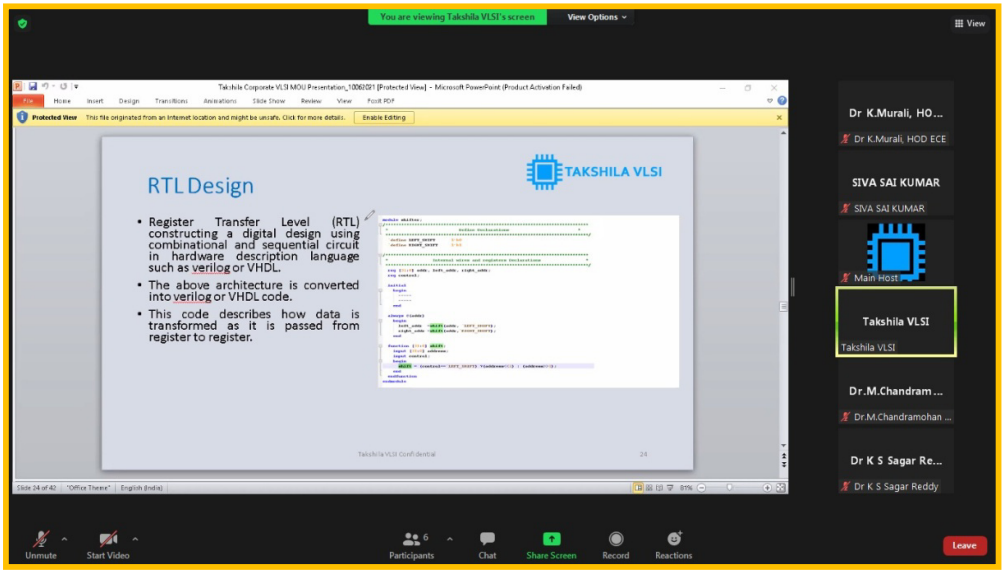
At present most of the software companies are establishing their own VLSI services. Some of the companies are Wipro, Infosys, HCL Technologies, L & T Infotech, Mindtree, etc. The various core job opportunities are as follows

- Physical design engineer
- STA engineer
- EM IR Sign off Engineer
- DFT Engineer
- Methodology & Flow Engineer
- Physical verification Engineer



Explaining about ASIC Design flow.

In RTL design we have to construct a circuit in hardware description language such as Verilog or VHDL.



Explaining about RTL design

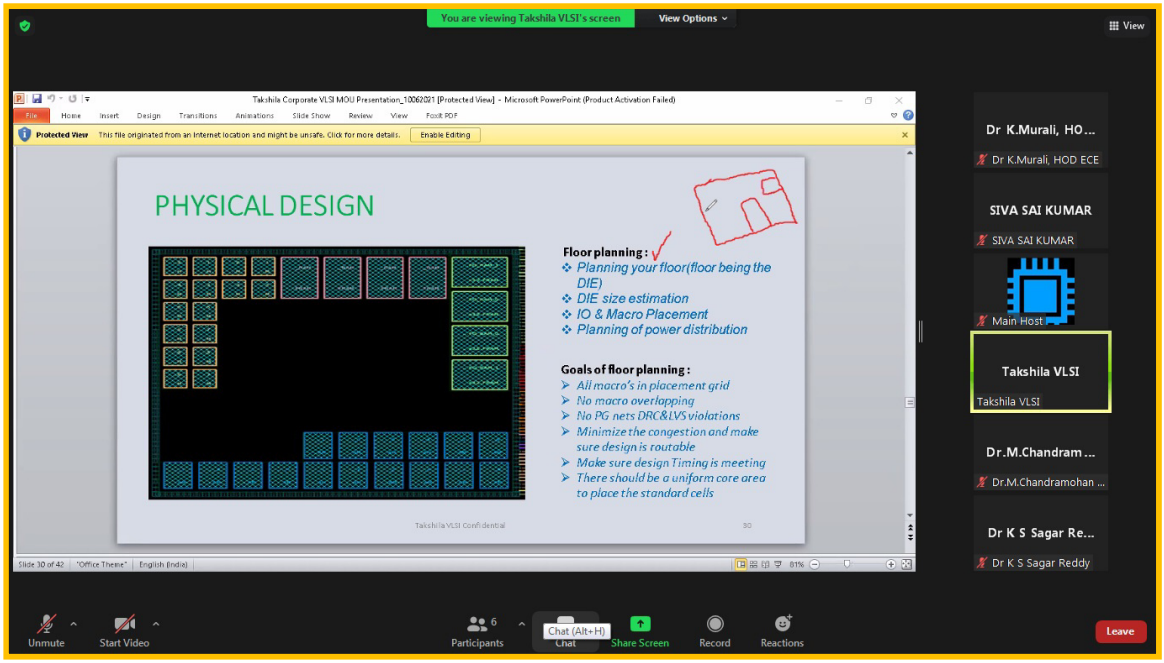
Design For Testability (DFT):

- Design For Testability (DFT) consists of IC design techniques that add testability features to a hardware product design.
- DFT is a technique, which facilitates a design to become testable after production.

- We will check the memory present in our design.
- Its the extra logic which we put in the normal design, during the design process, which helps its post-production testing.
- Post-production testing is necessary because, the process of manufacturing is not 100% error free.
- There are defects in silicon which contribute towards the errors introduced in the physical device.

The various inputs for physical design are

- Gate level Netlist
- Constraints
- Logic library
- Physical library
- For multi voltage domain designs

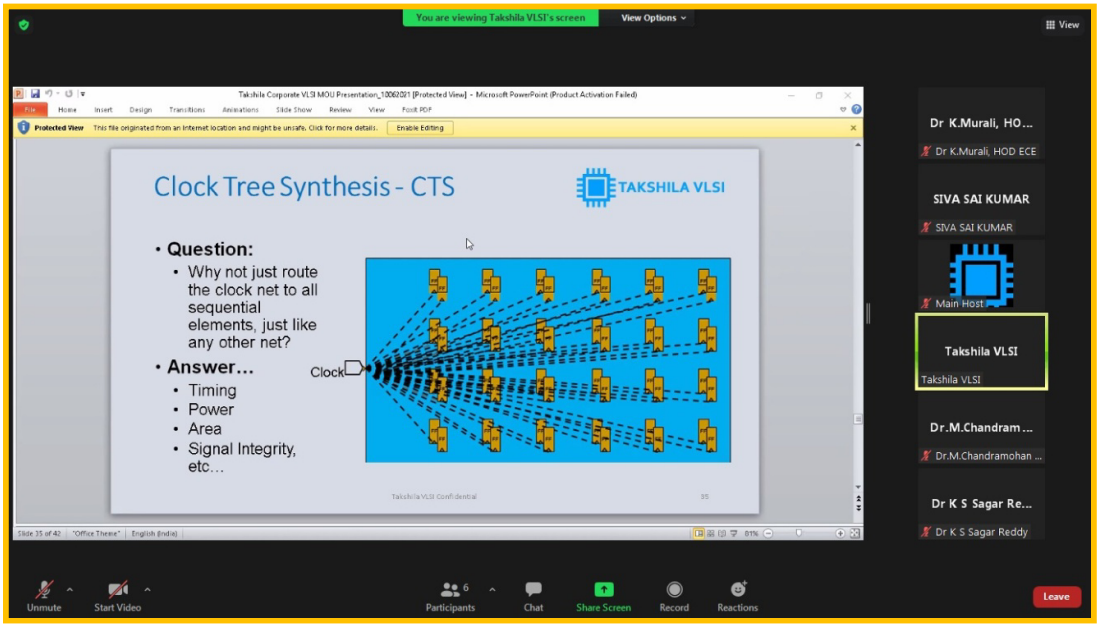


Explaining about physical design

Floorplanning – Full Chip:

Full chip floor planning goals:

- Estimation of die size by minimizing core area
- Planning the core area for different IPs in the chip (Like USB blocks, Video blocks, Display blocks, DDR blocks…)
- Planning of IO pads
- Power planning



Explaining about clock tree synthesis – CTS

Students asking queries

At the end Dr. K. Murali, HOD of ECE expressed gratitude to the resource person for giving valuable suggestions regarding various opportunities in VLSI design.

Total Number of participants:111